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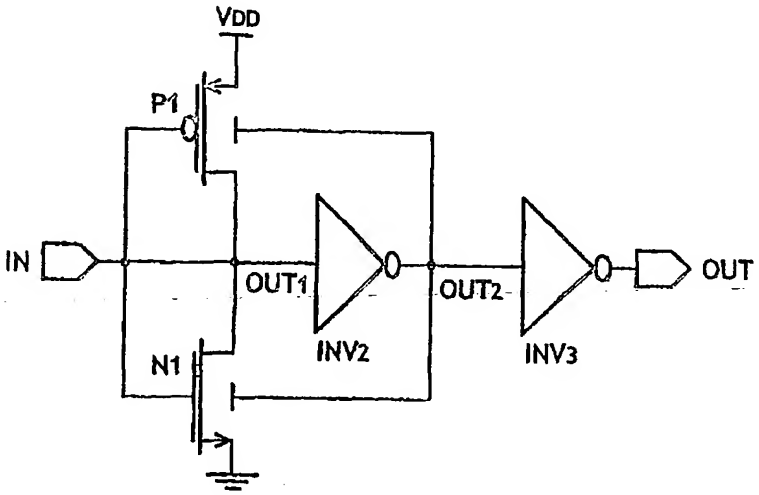
(54) Title: SCHMITT TRIGGER CIRCUIT IN SOI



(57) Abstract: This invention relates to a trigger circuit with hysteresis using the semiconductor on insulator technology, characterised in that it comprises at least two CMOS inverter stages, each inverter stage being composed of a first branch comprising at least one P-channel junction field effect transistor (PFET) in series between a first power supply potential VDD and an output node from the inverter stage, and a second branch comprising at least one N-channel junction field effect transistor (NFET) in series between the said output node from the inverter stage and a second power supply potential, the said transistors of each inverter stage having their grids connected together to receive an input signal, the input to each of the inverters directly or indirectly receiving the input signal of the said circuit, the output signal from the said circuit being obtained directly or indirectly by the output signal from one of the inverter stages and in that the substrate potential of each transistor of at least one inverter stage is dynamically controlled by a control signal output from the said circuit.

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